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# Modified Asymmetric Source Multilevel Inverter with Lower Number of Components

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***Abstract*— This study presents a particular design for staggered inverter that work in asymmetric source configuration. The proposed inverter can create flight of stairs yield voltage waveform that incorporates all voltage levels. The proposed inverter is contrasted and regular flowed staggered inverter regarding number of switches. Multicarrier sinusoidal heartbeat width balance conspires took on for producing exchanging signals. The viability of proposed particular staggered inverter is confirmed through simulation results.**

**Keywords—Multilevel inverter; less number of devices; sinusoidal pulse width modulation; total harmonic distortion**

## 1. Introduction

Multilevel inverters (MLI) have achieved increasing acceptance in high and medium power applications. Recently, for high power application, multilevel converters are widely used such as static var compensators, electric drives, active power filters and renewable energies application. The advantages of MLI are high quality output waveform, less harmonic distortion and better electromagnetic capability [1]– [6]. However, MLI have some demerits, that is, required number of power semiconductor switches along with circuit components such as gate driver circuit, protection circuit. This makes intricacy in circuit, more installation area, expensive and reduces the efficiency & reliability of the inverter. Generally, MLIs are classified in three topology as neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) [1]–[9]. Among the conventional topologies, CHB has received wide response because of its modular structure. However, CHB MLI required isolated dc voltage source is a limitation of the topology [7]. A CHB is classified in to two categories as symmetric and asymmetric MLI on the basis of magnitude DC voltage source. In symmetric MLI, the magnitudes of DC sources are equal, whereas in asymmetric MLI magnitudes of DC sources are unequal. Asymmetric MLI reduced the installation area and cost of inverter circuit. The asymmetric CHB MLI generates higher number of voltage step as compared to symmetric MLI with equal number of power semiconductor switches [7]

but switching scheme is complex and there is possibility to lose the modularity. A modular structure for symmetric MLI with less number of switches is addressed in this paper.

## 2. Proposed Circuit

This paper introduces a new topology of asymmetric multilevel modular with a new component arrangement, including 10 switches, 10 diodes, and 4 unequal dc sources (two $2V_{DC}$ and two $1V_{DC}$) named as Envelope type (E-type). This arrangement synthesizes voltage sources that produce 13 levels (6 positive levels, 6 negative levels, and zero level) without any additional circuit. The main concept of this circuit is to create different paths from different sides of a dc source to be connected to other sources. Fig. 4.1 shows the configuration of E-type asymmetrical module in where dc sources are located in the middle of the circuit and are connected together to form different voltage levels via surrounding switch ($S_1 - S_6$). A bidirectional switch ($S_7$) is required to avoid short circuit of dc sources on left or right sides of the module. Another bidirectional switch ($S_8$) is also needed to achieve the voltage levels of $\pm 5V_{dc}$. Different switching conditions of this structure are shown in Fig. 1 and Table 1.

As shown in Table 1, switch pairs ($S_1$,$S_4$) and ($S_2$,$S_3$) belong to positive and negative levels, respectively. In addition, ($S_1$,$S_2$) and ($S_3$,$S_4$) cannot be on at the same time. Fig. 4 shows the output voltage of the proposed inverter with the associated pulse pattern in one cycle of the fundamental voltage. As shown in Fig. 1, switches $S_1$, $S_2$, $S_3$, $S_4$, and $S_7$ are turned on and turned off in low frequency which reduces switching losses to a great extent. Other switches also operate in a reasonable switching frequency.

Fig. 1 shows all switching states of E-type module. The designing of the proposed module and their switching paths are smartly selected in such a way that there are no positive pole of dc links on the anode side of diode to conduct. Thus, diodes prevent short circuiting of the switches.

Table 1 Look-up table for switching state of proposed thirteen level inverter

| State | combined signal "$g_{comb}(t)$" | Output voltage | ON state switches |
|---|---|---|---|
| 1 | 6 | 6Vdc | $S_1$, $S_4$, $S_5$ |
| 2 | 5 | 5 Vdc | $S_1$, $S_4$, $S_8$ |
| 3 | 4 | 4 Vdc | $S_1$, $S_4$, $S_6$ |
| 4 | 3 | 3 Vdc | $S_1$, $S_5$, $S_7$ |

| | | | |
|---|---|---|---|
| 5 | 2 | 2 Vdc | $S_1$, $S_7$, $S_8$ |
| 6 | 1 | Vdc | $S_1$, $S_6$, $S_7$ |
| 7 | 0 | 0 | $S_1$, $S_3$, $S_5$ OR $S_2$, $S_4$, $S_6$ |
| 8 | -1 | - Vdc | $S_2$, $S_5$, $S_7$ |
| 9 | -2 | -2 Vdc | $S_2$, $S_5$, $S_8$ |
| 10 | -3 | -3 Vdc | $S_2$, $S_6$, $S_7$ |
| 11 | -4 | -4 Vdc | $S_2$, S3, $S_5$ |
| 12 | -5 | -5 Vdc | $S_2$, $S_3$, $S_8$ |
| 13 | -6 | -6 Vdc | $S_2$, $S_3$, $S_6$ |

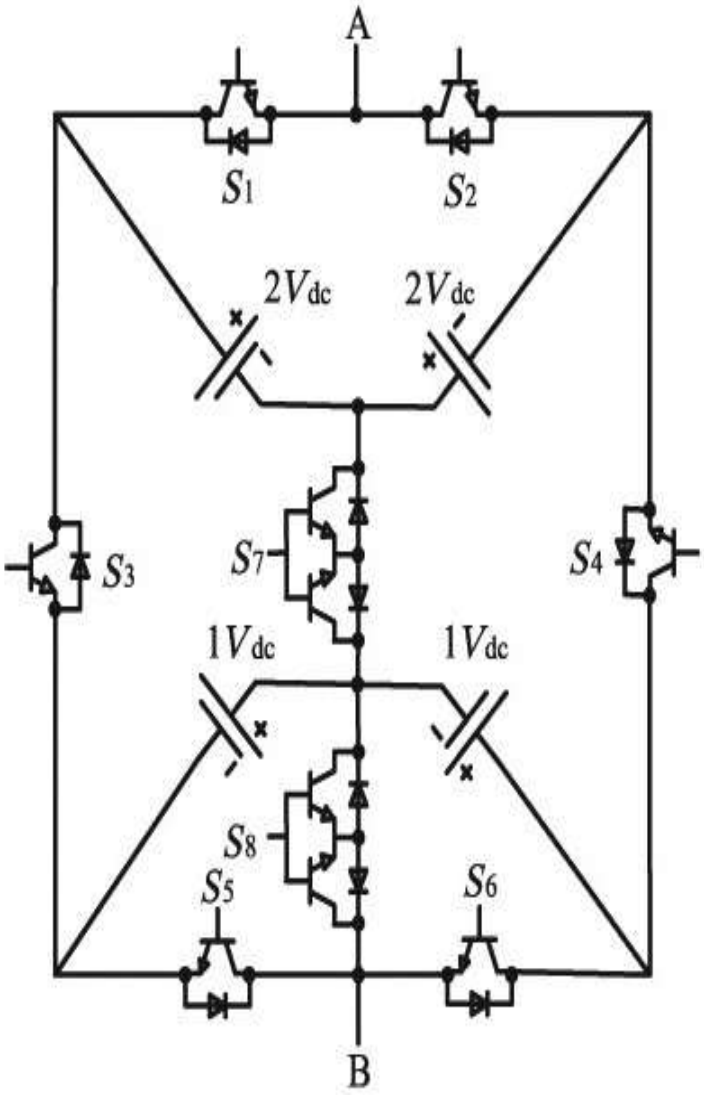



Fig. 1 Proposed E-type module of MLI

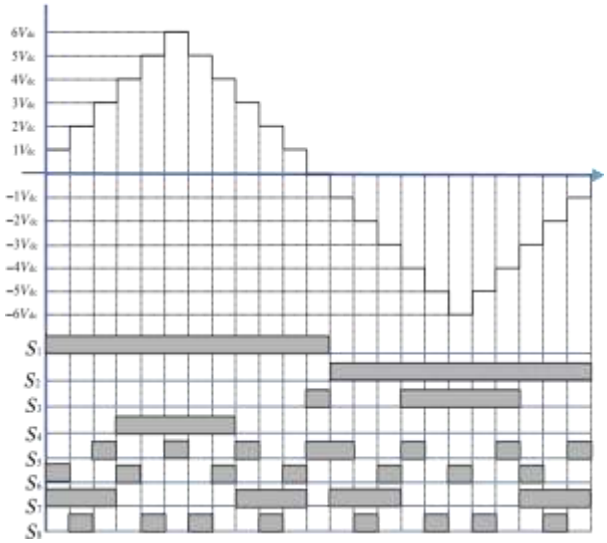
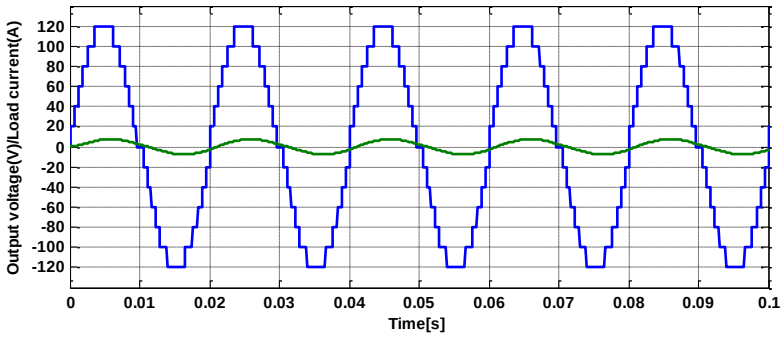


Fig. 4.2. Switching pattern of proposed converter in one cycle.

## 3. Simulation Results

To verify the performance of proposed configuration, a 13-level inverter has been simulated in MATLAB/Simulink version 2009a. The equivalent circuit of proposed 13-level asymmetrical inverter is shown in Fig. 1. It consists of four unequal DC voltage source having a magnitude of 40V, 40V, 20V and 20V respectively, which generates 13-level staircase output voltage waveform of maximum amplitude of 120V. A series RL branch considered as AC load at the output terminal. The output voltage and current waveforms for carrier frequency of 50 Hz and 2 kHz with their corresponding voltage harmonic spectrums are shown in Fig. 2. Harmonic spectrum observed THD 4.61% and 8.44% for 50 Hz and 2 kHz carrier frequency, respectively. Harmonic of output voltage has significant 4.61 % THD at 50Hz carrier frequency. It satisfies IEEE 519 1992 standard.




(a) Output voltage and load curent at 50 Hz carrier frequency

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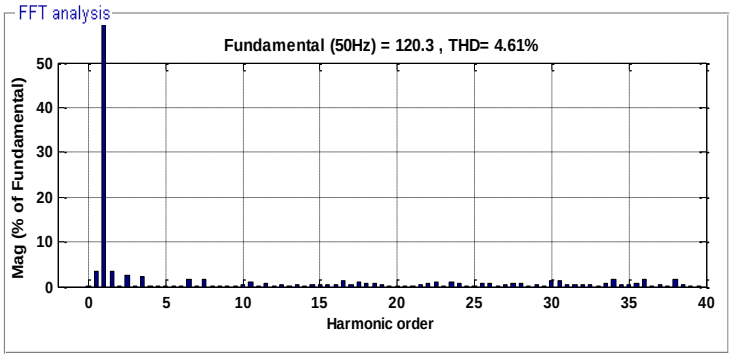
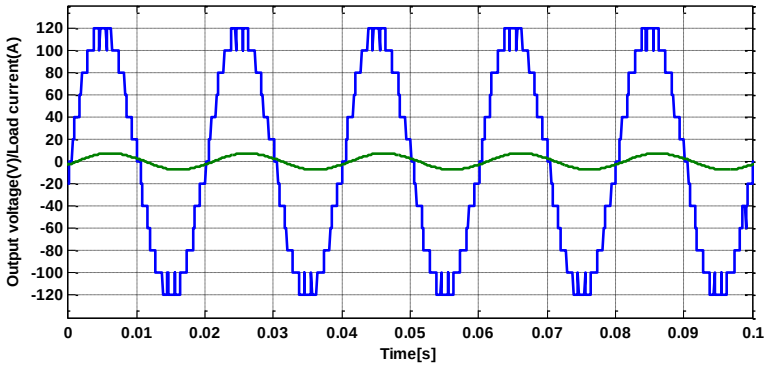
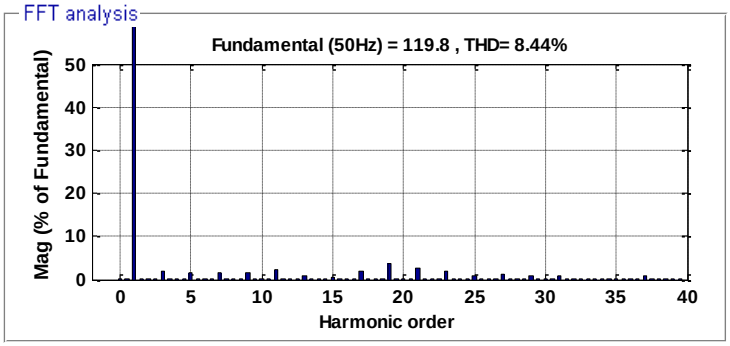



(b) Harmonic spectrum of output volatge at 50 Hz carrier frequency




(c) Output voltage and load curent at 2 kHz carrier frequency




(d) Harmonic spectrum of output volatge at 2 kHz carrier frequency

Fig. 2 Simulation results for 13-level inverter

## 4. Comparative Study

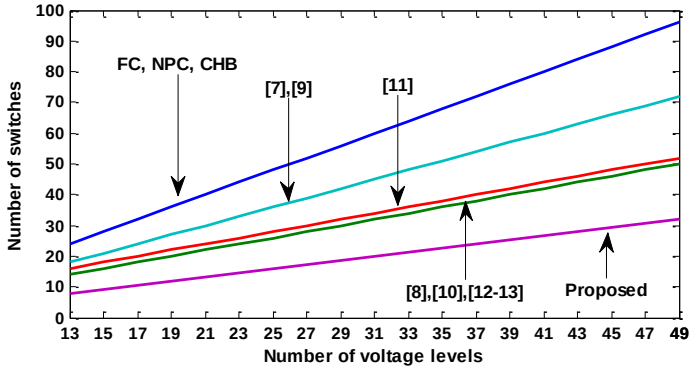
In this section, to show the benefits of proposed topology over the conventional and recent topologies reported in the Refs. 7-13, a comparative study is performed in terms of number of switches, dc sources, gate drivers and total standing voltage on switches. The main objective of this paper is to present a new structure for asymmetrical MLI which requires a lesser number of power semiconductor switches over the conventional

(FC, CHB, NPC) and other recent topologies. It can be seen from Table 2 that the number of power semiconductor switches and related gate drivers are significantly lower in the proposed inverter compared to the conventional and other recent topologies for same number of voltage levels as shown in Fig. 3(a). Therefore, installation area and cost of the proposed inverter will be lower than other MLIs. Table 2 also represents the total standing voltage (TSV) for the proposed topology has low TSV when compared to the recent topologies with same number of DC link voltage is shown in Fig. 3 (b).

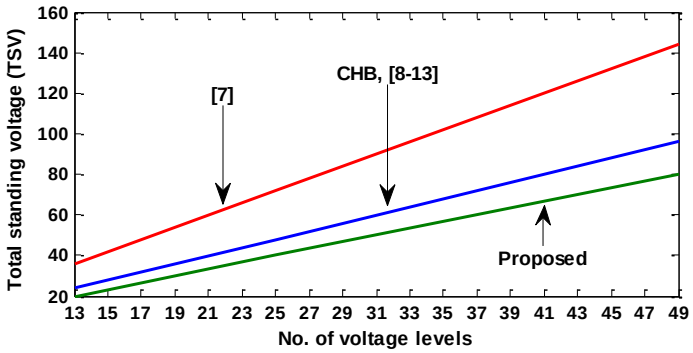
Table 2 Comparison between different multilevel inverter topologies

| Type of Topologies | No. of Switches | No. of DC sources (n) | No. of gate drivers | Total standing voltage (TSV*E) |
|---|---|---|---|---|
| FC | 4n | 6 | 4n | 4n |
| CHB | 4n | 6 | 4n | 4n |
| NPC | 4n | 6 | 4n | 4n |
| Ref. 7 | 2n+4 | 6 | 2n+4 | 6n |
| Ref. 8 | 2n+2 | 6 | 2n+2 | 4n |
| Ref. 9 | 5n+1 | 3 | 5n+1 | 8n |
| Ref. 10 | 2n+2 | 6 | 2n+2 | 4n |
| Ref. 11 | 3n | 6 | 3n | 4n |
| Ref. 12 | 2n+2 | 6 | 2n+2 | 4n |
| Ref. 13 | 2n+2 | 6 | 2n+2 | 4n |
| Proposed | 2n | 4 | 2n | 5n |

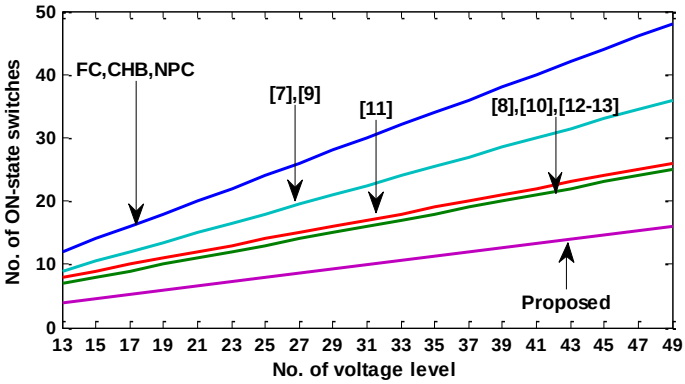
The ON-state switches in multilevel inverter leads to undesired voltage drop that causes power loss. Generally, half of the switches in multilevel inverter are in conduction state for an instant but in the proposed topology only three switches are conducting out of eight. Therefore, the number of ON-state switches are lower in the proposed topology as compared to contemporary topologies as shown in Fig. 3(c). Therefore, the total power loss of the proposed topology is reduced, and the efficiency of the inverter is improved.




(a) No. of output voltage level verses number of switches




(b) No. of output voltage level verses number of ON-state switches




(c) No. of output voltage level verses total standing voltage (TSV)

Fig. 4.5 Comparison between topologies based on different parameters

## 5. Conclusion

This paper presented a new MLI topology that can generate 13 levels with reduced components. It can be used in high-voltage high-power applications with unequal dc sources. As can be easily modularized, it can be used in cascade

arrangements to form high-voltage outputs with low stress on semiconductors and lowering the number of devices. Modular connection of these modules leads to achieve more voltage levels with different possible paths. It causes an improvement in the reliability of the of proposed module is its ability to generate both positive and negative output voltages without any H-bridge circuit at the output of the inverter. THD% is 3.46% and 4.54% in simulation and experimental results, respectively, that satisfy harmonics standard (IEEE519). Also, module is tested in three different frequencies and under different resistive–inductive loads that results shows good performance.

## References

1. A. Nabae, I. Takahashi and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Trans. Industry Appl.*, vol. IA-17, no. 5, pp. 518-523, Sept. 1981.
2. Y. Cheng, C. Qian, M.L. Crow, S. Pekarek, S. Atcitty, "A comparison of diode-clamped and cascaded multilevel converters for a STATCOM with energy storage," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1512–1521, 2006
3. S. De, D. Banerjee, K. Siva Kumar, K. Gopakumar, R. Ramchand, C. Patel, "Multilevel inverters for low-power application," *IET Power Electron.*, vol. 4, no. 4, pp. 384–392, 2011
4. K. Thakre, K. B. Mohanty, H. Ahmed, A. K. Nayak, "Modified Cascaded Multilevel Inverter with Reduced Component Count", 14th IEEE India Council International Conference 2017 (INDICON), IIT Roorkee, India, 15-17 Dec. 2017
5. K. Thakre, K. B. Mohanty, A. K. Nayak, R. N. Mishra, "Design and Implementation of Symmetric and Asymmetric Structure for Multilevel Inverter", 8th IEEE National Power Electronics Conference (NPEC), College of Engineering Pune, India, 18-20 Dec., 2017, pp. 31-37
6. R. Rabinovici, D. Baimel, J. Tomasik, A. Zuckerberger, "Thirteen-level cascaded H-bridge inverter operated by generic phase shifted pulse-width modulation," *IET Power Electron.*, 2013, vol. 6, no. 8, pp. 1516 1529
7. A. Ajami, M. Jannati Oskuee, M. Khosroshahi and A. Mokhberdoran, "Cascade-multi-cell multilevel converter with reduced number of switches," *IET Power Electronics*, vol. 7, no. 3, pp. 552-558, March 2014.
8. A.K. Sadigh, V. Dargahi, M. Abarzadeh, S. Dargahi, "Reduced DC voltage source flying capacitor multicell multilevel inverter: analysis and implementation," *IET Power Electron.*, vol. 7, no. 2, pp. 439 450, 2014

9. A.K. Panda, Y. Suresh, "Performance of cascaded multilevel inverter by employing single and three-phase transformers," *IET Power Electronics*, vol. 5, no. 9, pp. 1694-1705, November 2012.
10. A. Ajami, M. R .J. Oskuee, M. T. Khosroshahi, et al., Cascade multi-cell multilevel converter with reduced number of switches, *IET Power Electron*. **7** (2014) 552–558.
11. M. F. Kangarlu, E. Babaei, M. Sabahi, Cascaded cross-switched multilevel inverter in symmetric and asymmetric conditions, *IET Power Electron.* **6** (2013) 1041-1050.
12. Y. Ounejjar, K. Al-Haddad, L. A. Grégoire, Packed U Cells Multilevel Converter Topology: Theoretical Study and Experimental Validation, *IEEE Trans. Ind. Electron.* **58** (2011) 1294–1306
13. Z. Du, L. M. Tolbert, J. N. Chiasson, and B. Ozpineci, "Reduced switching-frequency active harmonic elimination for multilevel converters," IEEE Trans. Ind. Electron. , vol. 55, no. 4, pp. 1761–1770, Apr. 2008.
14. M. Perez, S. Kouro, J. Rodriguez, and B. Wu, "Modified staircase modulation with low input current distortion for multicell converters," in Proc. IEEE Power Electron. Spec. Conf. , Jun. 2008, pp. 1989–1994.
15. M. G. Hosseini Aghdam, S. H. Fathi, and G. B. Gharehpetian, "Elimination of harmonics in a multi-level inverter with unequal DC sources using the homotopy algorithm," in Proc. IEEE ISIE , Jun. 2007, pp. 578–583.
16. V. G. Agelidis, A. I. Balouktsis, and M. S. A. Dahidah, "A five-level symmetrically defined selective harmonic elimination PWM strategy: Analysis and experimental validation," IEEE Trans. Power Electron. , vol. 23, no. 1, pp. 19–26, Jan. 2008
17. A. Nami, F. Zare, A. Ghosh, F. Blaabjerg, "A hybrid cascade converter topology with series-connected symmetrical and asymmetrical diode-clamped H-bridge cells," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 51–65, 2011
18. M. Veenstra, A. Rufer, "Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives," *IEEE Trans. Ind. Appl.*, vol. 41, no. 2, pp. 655–664, 2005
19. K.K Gupta, S. Jain, "Comprehensive review of a recently proposed multilevel inverter," *IET Power Electron.*, vol. 7, no. 3, pp. 467–479, 2014.
20. K. Thakre and K. B. Mohanty, "Comparative analysis of THD for symmetrical and asymmetrical 17 level cascaded H-bridge inverter using carrier based PWM techniques," Proc In: *IEEE Int. Conf. on Industrial Instrumentation and Control (ICIC),* Pune, India, 2015, pp.306-31

21. K. Thakre, K. B. Mohanty, V. S. Kommukuri, and A. Chatterjee, New Topology for Asymmetrical Multilevel Inverter: An Effort to Reduced Device Count, *Journal of Circuit System & Computers*, 27(4), 1850055, (2018).
22. K. Thakre, K. B. Mohanty, & A. Chatterjee, "Reduction of circuit devices in symmetrical voltage source multilevel inverter based on series connection of basic unit cells" *Alexandria Engineering Journal (Elsevier)*, vol. 57, no. 4 pp. 2703-2712, 2018.
23. K. Thakre, K.B. Mohanty, V.S. Kommukuri, and A. Chatterjee, A modified circuit for symmetric and asymmetric multilevel inverter with reduced components count, *Int. Trans. Elect. Energy Systems*, 29(6), e12011, (2019).
24. K. Thakre, K. B. Mohanty, & A. Chatterjee, "Modeling and Simulation of an Asymmetrical Modular Multilevel Inverter with Less Number of Components", *European Jour. Power Electronics (Taylor & Francis),* vol. 30, no. 2 pp. 69-79, 2020